1448303

PATENT SPECIFICATION

(11) 1448303

(21) Application No. 23735/74 (22) Filed 29 May 1974
(31) Convention Application No. 2336821 (32) Filed 19 July 1973 in (19)
(33) Germany (DT)
(44) Complete Specification published 2 Sept. 1976
(51) INT CL² H01L 29/78
(52) Index at acceptance
H1K 217 223 22Y 312 422 42X 51Y 52X 543 54Y 551 55Y 57Y 581

(54) IMPROVEMENTS IN OR RELATING TO TRANSISTOR ARRANGEMENTS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

The present invention relates to transistor arrangements in which two field-effect transistors are integrated in a semiconductive layer on an insulating substrate.

According to the invention, there is provided a semiconductor arrangement comprising two field-effect transistors integrated in a layer of semiconductor material on an insulating substrate, said transistors having a common channel zone covered by a common gate insulating layer with a common gate electrode located thereon, the source and drain zones of one transistor lying opposite to one another on a first axis lying parallel to the surface of said layer, and the source and drain zones of the other transistor lying opposite to one another on a second axis lying parallel to the surface of said layer and at an angle to said first axis. The two axes are conveniently substantially at right-angles to one another.

An advantage of the transistor arrangement in accordance with the invention is that, as a result of the integration of the two transistors, they utilise only about two-thirds of the surface area of the semiconductor layer which would be required in an arrangement in which the two field-effect transistors were arranged next to one another.

When the transistor arrangement in accordance with the invention is employed for storage purposes, a reduction in cost is achieved because it is possible to accommodate considerably more storage elements on one semiconductor chip than is possible with conventional storage arrangements.

In a preferred embodiment of the invention, the two transistors are of different conductivity types, one transistor being a "deep depletion" transistor. An advantage of this arrangement is that, in every case, one of the two transistors of the transistor arrangement will always be conductive whilst the other transistor blocks.

The invention will now be further described with reference to the drawings, in which:—

Figure 1 is a schematic plan view of a transistor arrangement according to the invention;

Figure 2 is a section taken along the line II—II of Figure 1, showing one transistor in the blocked state;

Figure 3 is a section taken along the line III—III of Figure 1, showing the other transistor in the conductive state;

Figure 4 is a similar view to that of Figure 2 showing the one transistor in the conductive state;

Figure 5 is a similar view to that of Figure 3, showing the other transistor in the blocked state;

Figure 6 is a circuit symbol of a transistor arrangement according to the invention;

Figure 7 is a circuit diagram of a transistor arrangement in accordance with the invention in which a double transistor is used as a storage device; and

Figure 8 is a circuit diagram of another transistor arrangement in accordance with the invention in which a double transistor is used as a storage device.

Referring to Figure 1, a transistor arrangement according to the invention comprises a double transistor comprising two integrated field-effect transistors with a common channel zone 1. One transistor 52 of the double transistor comprises source and drain zones 5 and 51 respectively and the common channel zone 1, whilst the other transistor 42 comprises source and drain zones 4 and 41 respectively and the common channel zone 1. The transistor 42 lies along an axis parallel to the surface of the semiconductor layer which forms approximately a right-angle with the similar axis along which the transistor 52 lies.

Figure 2 is a side-sectional view of the transistor 42 comprising the source and drain zones 4 and 41 and the channel zone 1. The

whole transistor arrangement is formed in a semiconductor arranged on an electrically insulating substrate 6. Preferably, this electrically insulating substrate consists of sapphire or spinel. On the substrate 6 there is arranged a semiconductor layer, preferably a monocrystalline silicon layer. The thickness of this layer is preferably such that an inversion layer formed therein occupies substantially the entire thickness of the layer.

The source zone and drain zones 4 and 41 are formed by diffusion in this monocrystalline silicon layer, the channel zone 1 being arranged between these two zones. As shown in Figure 2, a common gate insulating layer 2, which may consist, for example, of SiO_2 or Si_3N_4, is arranged above the common channel zone 1. Preferably, however, the gate insulating layer consists of a SiO_2 layer with a Si_3N_4 layer arranged upon it (MNOS technique) or of a SiO_2 layer with an Al_2O_3 layer arranged upon it (MAOS technique). A common gate electrode 3 is applied to the gate insulating layer. The source zone 4 is provided with an electrode 43 having a contact 44 and the drain zone 41 with an electrode 45 having a contact 46. The gate electrode 3 is provided with a contact 31.

Figure 3 shows a cross-section through the other transistor 52 which comprises the source and drain zones 5 and 51 and the channel zone 1. The source and the drain zones 5 and 55 and the channel zone 1 are arranged on the substrate 6 in the semiconductor layer preferably consisting of monocrystalline silicon, as was the transistor of Figure 2. The zones 5 and 55 are again produced by diffusion into the semiconducttor layer. The zone 5 is provided with an electrode 53 having a contact 54, and the zone 51 with an electrode 55 having a contact 66.

Preferably, the common channel zone 1 is n^- doped, the source and drain zones 4 and 41 are p^+-doped and the source and drain zones 5 and 51 are n^+-doped. When the individual zones are doped in this way, the transistor 42 represents a p-type transistor and the transistor 52 represents an n-type transistor of the deep-depletion type. Alternatively, the channel zone can be p^--doped, in which case the p-type transistor 42 is of the deep-depletion type.

The mode of operation of the transistor arrangement in accordance with the invention illustrated will now be explained with reference to Figures 2, 3, 4 and 5. When a positive voltage $+Ug$ is applied to the gate contact 31, an n-conductive enrichment layer 7 is formed in the channel zone 1. This results in the transistor 52 (Figure 3) being conductive since the two n^+-zones 5 and 51 are then connected by the n^--enrichment layer 7. In this case, however, the transistor 42 is blocked, since the two p^+-zones 4 and 41 are isolated from one another by the p-n junctions (Figure 2).

If a negative voltage $-Ug$ is applied to the gate contact 31, a p-conductive channel is formed in the channel zone 1. In Figures 4 and 5 this p-conductive channel is indicated at 8. The formation of a p-conductive channel results in the two p^+—zones 4 and 41 of the transistor 42 (Figure 4) being conductively connected to one another, whilst, in comparison, the two n^+-zones 5 and 51 of the transistor 52 (Figure 5) are now isolated from one another since two p-n junctions are present between them and a depletion zone is formed beneath the p-conductive channel which zone extends to the insulating substrate. In this example, the transistor 42 of the p-type and the transistor 52 is a so-called deep depletion transistor of the n-type.

Thus, at a specific gate voltage, as described above, at all times only one of the two transistors is in the conductive state, which is a fact of great advantage for use in digital circuits. If both the n-channel and the p-channel transistor are to possess approximately the same internal resistance in the conductive state, the ratio of the lengths of the sides of the rectangular channel zone is selected to be equal to the root of the ratio of the average mobilities of the two charge carrier types $\sqrt{\mu_p : \mu_n}$. In this case, the saving in area obtained by using the double transistor as compared with the area required for two transistors arranged next to one another, is approximately 40%.

Figure 6 shows a circuit symbol for a transistor arrangement in accordance with the invention. The gate electrode terminal 31 is common to the two transistors. The source and drain terminals are indicated at 44 and 46 respectively, of the transistor 42, and the source and drain terminals of the transistor 52 at 54 and 56 respectively.

Figure 7 shows a circuit including a transistor arrangement in accordance with the invention. The circuit may represent, for example, an associative storage element using the MNOS technique or the MAOS technique. The storage element is selected by means of a selector transistor 9. For this purpose the gate terminal of the transistor 9 is connected to a word line 10. The actual storage transistor is a transistor arrangement 11 in accordance with the invention, in which the gate insulator layer may, for example, be formed using the MNOS technique, or the MAOS technique, in the usual fashion. On readout of the stored item of data, "0" or "1", one path in the transistor arrangement of the invention is always conductive. Therefore current always flows on one of two digit lines 12 and 13.

The storage element illustrated in Figure 7 is noteworthy for its high interference resistance.

Figure 8 shows a further example of a circuit representing an associative storage element using a transistor arrangement in accordance with the invention. In this case, this is an associative fixed word store. The items of information are stored in a transistor arrangement 14 in accordance with the invention by means of a word line 18. On read-out of the information, a transistor 15 and the transistor arrangement 14 of the invention act as a coincidence circuit. Only when the items of information interrogated via one of the digit lines 16 and 17 is identical with an item of information stored in the transistor arrangement 14 is the transistor 15 in the blocked state.

WHAT WE CLAIM IS:—

1. A transistor arrangement comprising two field-effect transistors integrated in a layer of semiconductor material on an insulating substrate, said transistors having a common channel zone covered by a common gate insulating layer with a common gate electrode located thereon, the source and drain zones of one transistor lying opposite to one another on a first axis lying parallel to the surface of said layer, and the source and drain zones of the other transistor lying opposite to one another on a second axis lying parallel to the surface of said layer and at an angle to said first axis.

2. An arrangement as claimed in Claim 1, wherein said axes are substantially at right-angles to one another.

3. An arrangement as claimed in Claim 1 or Claim 2, wherein said insulating substrate consists of spinel.

4. An arrangement as claimed in Claim 1 or Claim 2, wherein said insulating substrate consists of sapphire.

5. An arrangement as claimed in any one of the preceding Claims, wherein said semiconductor layer consists of silicon.

6. An arrangement as claimed in any one of the preceding Claims, wherein the gate insulating layer consists of an SiO_2 layer and/or an Si_3N_4 layer.

7. An arrangement as claimed in any one of Claims 1 to 5, wherein the gate insulating layer consists of a layer of SiO_2 and a layer of Al_2O_3.

8. An arrangement as claimed in any one of the preceding Claims, wherein said common channel zone is n^--doped or p^--doped, the source and drain zones of one of said transistors are p^+-doped and the other source and drain zones of the other said transistors are n^+-doped.

9. A transistor arrangement substantially as hereinbefore described with reference to and as shown in Figures 1 to 5 of the drawings.

10. An associative storage element comprising a transistor arrangement as claimed in any one of the preceding Claims, and a selector field-effect transistor, wherein the said selector transistor is controllable via a word line, wherein said transistor arrangement is connected in series with said selector transistor, wherein the source or drain terminal of said selector transistor is connected in series with the parallel-connected drain or source terminals of the respective transistors of said transistor arrangement, wherein the common gate electrode of said transistor arrangement is connected to said word line; and wherein a separate digit line is connected to the remaining drain or source terminal of each transistor of said transistor arrangement.

11. An associative storage element comprising a transistor arrangement as claimed in any one of Claims 1 to 9, wherein the gate of a further field-effect transistor is connected to the parallel-connected source or drain terminals of the two transistors of said transistor arrangement, wherein a separate digit line is connected to the remaining drain or source terminal of each of the transistors of said transistor arrangement; and wherein the common gate electrode of said transistor arrangement is connected to a word line, the arrangement being such that said further transistor is in the blocked state when there is coincidence between the item of information stored in said transistor arrangement and the states prevailing on said digit lines.

12. An associative storage element substantially as hereinbefore described with reference to and as shown in Figure 7, or Figure 8, of the drawings.

For the Applicants,
G. F. REDFERN & CO.,
St. Martin's House,
177 Preston Road,
Brighton, Sussex.
and
High Holborn,
London, W.C.1.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1976.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1448303 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

Fig.1

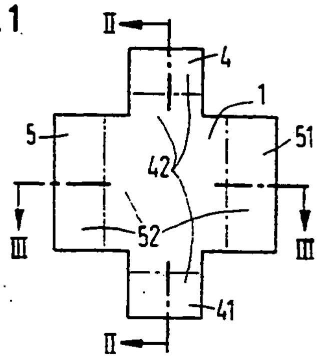

Fig.6

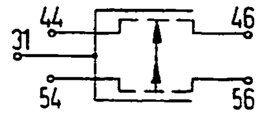

Fig.2

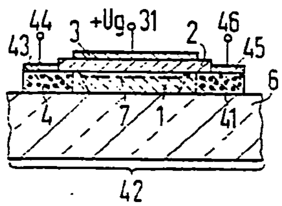

Fig.3

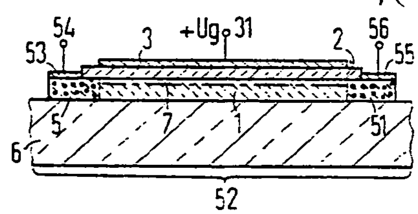

Fig.4

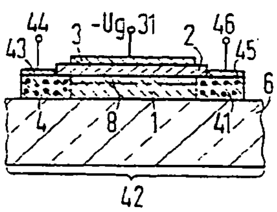

Fig.5

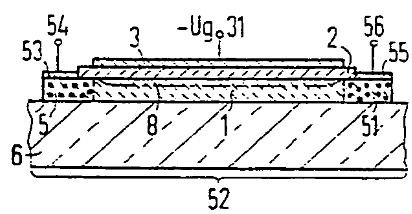

Fig. 7

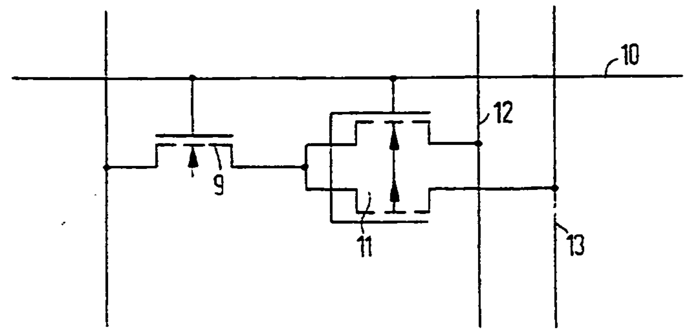

Fig. 8